This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Canceled)

2. (Currently Amended) ~~The~~ A semiconductor layer structure comprising: ~~as claimed in Claim 1,~~

a relaxed $Si_{1-x}Ge_x$ layer; wherein said relaxed $Si_{1-x}Ge_x$ layer is doped either partially or wholly p-type,

a bottom $Si_{1-z}Ge_z$ buffer layer on top of said relaxed $Si_{1-x}Ge_x$ layer;

a tensile tensile-strained Si quantum well layer on top of said bottom $Si_{1-z}Ge_z$ buffer layer;

a top $Si_{1-m}Ge_m$ buffer layer on top of said tensile tensile-strained Si quantum well layer; and,

a Si cap layer under tensile strain on top of said top $Si_{1-m}Ge_m$ buffer layer,

wherein said relaxed bottom $Si_{1-z}Ge_z$ buffer layer, tensile-strained Si quantum well layer, and top $Si_{1-m}Ge_m$ buffer layer and Si cap layer are substantially undoped.

3. (Original) The semiconductor layer structure as claimed in Claim 2, wherein the p-type portion of said relaxed $Si_{1-x}Ge_x$ layer has a dopant concentration between 10^{15} cm^{-3} and 10^{19} cm^{-3} and said relaxed $Si_{1-x}Ge_x$ layer has a Ge concentration x and relaxation, r, such that the in-plane lattice constant is 0.8-2.4% larger than that of bulk Si.

4. (Original) The semiconductor layer structure as claimed in Claim 3, wherein:

said bottom $Si_{1-z}Ge_z$ buffer layer is substantially lattice-matched to said relaxed $Si_{1-x}Ge_x$ layer and has a thickness ranging between 2 nm to 50 nm;

said tensile tensile-strained Si quantum well layer has a thickness ranging between 2 nm to 30 nm; and

said top $Si_{1-m}Ge_m$ buffer layer is substantially lattice-matched to said bottom $Si_{1-z}Ge_z$ buffer layer and has a thickness ranging between 2 nm to 20 nm.

5. (Original) The semiconductor layer structure as claimed in Claim 4, wherein said relaxed $Si_{1-x}Ge_x$ layer is formed on top of an insulating layer.

6. (Currently Amended) A ~~The~~ semiconductor layer structure comprising: ~~as claimed in Claim 1,~~

a relaxed $Si_{1-x}Ge_x$ layer; wherein said relaxed $Si_{1-x}Ge_x$ layer is doped either partially or wholly p-type,

a bottom $Si_{1-z}Ge_z$ buffer layer on top of said relaxed $Si_{1-x}Ge_x$ layer;

a tensile tensile-strained Si quantum well layer on top of said bottom $Si_{1-z}Ge_z$ buffer layer;

a top $Si_{1-m}Ge_m$ buffer layer on top of said tensile tensile-strained Si quantum well layer; and,

a Si cap layer under tensile strain on top of said top $Si_{1-m}Ge_m$ buffer layer,

wherein a portion of said top $Si_{1-m}Ge_m$ or bottom $Si_{1-z}Ge_z$ buffer layer or both top and bottom buffer layers adjacent to said Si quantum well is substantially undoped and a portion or entirety of the remaining regions of said bottom $Si_{1-z}Ge_z$ buffer layer or top $Si_{1-m}Ge_m$ buffer

layer or both buffer layers is doped n-type with a concentration ranging between $10^{17}cm^{-3}$ to 10^{21} cm^{-3}.

7. (Original) The semiconductor layer structure as claimed in Claim 6, where the thickness of the undoped portion of said bottom $Si_{1-z}Ge_z$ buffer layer or top $Si_{1-m}Ge_m$ buffer layer or both buffer layers adjacent to said Si quantum well is at least 0.5 nm.

8. (Original) The semiconductor layer structure as claimed in Claim 6, wherein the p-type portion of said relaxed $Si_{1-x}Ge_x$ layer has a dopant concentration between 10^{15} cm^{-3} and 10^{19} cm^{-3} and said relaxed $Si_{1-x}Ge_x$ layer has a Ge concentration x and relaxation, r, such that the in-plane lattice constant is 0.8-2.4% larger than that of bulk Si.

9. (Original) The semiconductor layer structure as claimed in Claim 6, wherein:

said bottom $Si_{1-z}Ge_z$ buffer layer is substantially lattice-matched to said relaxed $Si_{1-x}Ge_x$ layer and has a thickness ranging between 2 nm to 50 nm;

said tensile tensile-strained Si quantum well layer has a thickness ranging between 2 nm to 30 nm;

said top $Si_{1-m}Ge_m$ buffer layer is substantially lattice-matched to said bottom $Si_{1-z}Ge_z$ buffer layer and has a thickness ranging between 2 nm to 20 nm.

10. (Original) The semiconductor layer structure as claimed in Claim 9, wherein said relaxed $Si_{1-x}Ge_x$ layer is formed on top of an insulating layer.

11. (Canceled)

12. (Currently Amended) ~~The~~ A semiconductor layer structure comprising: ~~as claimed in Claim 11,~~

a relaxed $Si_{1-x}Ge_x$ layer; wherein said relaxed $Si_{1-x}Ge_x$ layer is doped either partially or wholly p-type,

an interposer $Si_{1-y}Ge_y$ layer on top of said relaxed $Si_{1-x}Ge_x$ layer;

a bottom $Si_{1-z}Ge_z$ buffer layer on top of said interposer $Si_{1-y}Ge_y$ layer;

a tensile tensile-strained Si quantum well layer on top of said bottom $Si_{1-z}Ge_z$ buffer layer;

a top $Si_{1-m}Ge_m$ buffer layer on top of said tensile tensile-strained Si quantum well layer;

a Si cap layer under tensile strain on top of said top $Si_{1-m}Ge_m$ buffer layer,

wherein said relaxed bottom $Si_{1-z}Ge_z$ buffer layer, tensile-strained Si quantum well layer, top $Si_{1-m}Ge_m$ buffer layer and Si cap layer are substantially undoped.

13. (Currently Amended) The semiconductor layer structure as claimed in Claim ~~11~~ 12, wherein the p-type portion of said relaxed $Si_{1-x}Ge_x$ layer has a dopant concentration between 10^{15} cm^{-3} and 10^{19} cm^{-3} and said relaxed $Si_{1-x}Ge_x$ layer has a Ge concentration x and relaxation, r, such that the in-plane lattice constant is 0.8-2.4% larger than that of bulk Si.

14. (Original) The semiconductor layer structure as claimed in Claim 13, wherein:

said interposer $Si_{1-y}Ge_y$ layer has Ge concentration, y, in the range of 0 to 20%, and thickness less than 5 nm;

said bottom $Si_{1-z}Ge_z$ buffer layer is substantially lattice-matched to said relaxed $Si_{1-x}Ge_x$ layer and has a thickness ranging between 2 nm to 50 nm;

said tensile tensile-strained Si quantum well layer has a thickness ranging between 2 nm to 30 nm; and,

said top $Si_{1-m}Ge_m$ buffer layer is substantially lattice-matched to said bottom $Si_{1-z}Ge_z$ buffer layer and has a thickness ranging between 2 nm to 20 nm.

15. (Original) The semiconductor layer structure as claimed in Claim 14, wherein said relaxed $Si_{1-x}Ge_x$ layer is formed on top of an insulating layer.

16. (Currently Amended) <u>A</u> ~~The~~ semiconductor layer structure <u>comprising:</u> ~~as claimed in Claim 11,~~

<u>a relaxed $Si_{1-x}Ge_x$ layer; wherein said relaxed $Si_{1-x}Ge_x$ layer is doped either partially or wholly p-type,</u>

<u>an interposer $Si_{1-y}Ge_y$ layer on top of said relaxed $Si_{1-x}Ge_x$ layer;</u>

<u>a bottom $Si_{1-z}Ge_z$ buffer layer on top of said interposer $Si_{1-y}Ge_y$ layer;</u>

<u>a tensile tensile-strained Si quantum well layer on top of said bottom $Si_{1-z}Ge_z$ buffer layer;</u>

<u>a top $Si_{1-m}Ge_m$ buffer layer on top of said tensile tensile-strained Si quantum well layer;</u>

<u>a Si cap layer under tensile strain on top of said top $Si_{1-m}Ge_m$ buffer layer,</u>

wherein a portion of said bottom $Si_{1-z}Ge_z$ buffer layer or top $Si_{1-m}Ge_m$ buffer layer or both buffer layers adjacent to said Si quantum well is substantially undoped and a portion or entirety of the remaining regions of said bottom $Si_{1-z}Ge_z$ buffer layer or top $Si_{1-m}Ge_m$ buffer layer or both buffer layers is doped n-type with a concentration ranging between $10^{17} cm^{-3}$ to $10^{21} cm^{-3}$.

17. (Original) The semiconductor layer structure as claimed in Claim 16, where the thickness of the undoped portion of said bottom $Si_{1-z}Ge_z$ buffer layer or top $Si_{1-m}Ge_m$ buffer layer or both buffer layers adjacent to said Si quantum well is at least 0.5 nm.

18. (Original) The semiconductor layer structure as claimed in Claim 16, wherein the p-type portion of said relaxed $Si_{1-x}Ge_x$ layer has a dopant concentration between 10^{15} cm^{-3} and 10^{19} cm^{-3} and said relaxed $Si_{1-x}Ge_x$ layer has a Ge concentration x and relaxation, r, such that the in-plane lattice constant is 0.8-2.4% larger than that of bulk Si.

19. (Original) The semiconductor layer structure as claimed in Claim 14, wherein:

said interposer $Si_{1-y}Ge_y$ layer has Ge concentration, y, in the range of 0 to 20%, and thickness less than 5 nm;

said bottom $Si_{1-z}Ge_z$ buffer layer is substantially lattice-matched to said relaxed $Si_{1-x}Ge_x$ layer and has a thickness ranging between 2 nm to 50 nm;

said tensile tensile-strained Si quantum well layer has a thickness ranging between 2 nm to 30 nm;

said top $Si_{1-m}Ge_m$ buffer layer is substantially lattice-matched to said bottom $Si_{1-z}Ge_z$ buffer layer and has a thickness ranging between 2 nm to 20 nm.

20. (Original) The semiconductor layer structure as claimed in Claim 19, wherein said relaxed $Si_{1-x}Ge_x$ layer is formed on top of an insulating layer.

21. (Canceled)

22. (Currently Amended) ~~The~~ A semiconductor layer structure comprising: ~~as claimed in Claim 21,~~

a relaxed $Si_{1-x}Ge_x$ layer; wherein said relaxed $Si_{1-x}Ge_x$ layer is doped either partially or wholly n-type,

a bottom $Si_{1-z}Ge_z$ buffer layer on top of said relaxed $Si_{1-x}Ge_x$ layer;

a compressive-strained $Si_{1-v}Ge_v$ quantum well layer on top of said bottom $Si_{1-z}Ge_z$ buffer layer;

a top $Si_{1-m}Ge_m$ buffer layer on top of said compressive-strained Si quantum well layer;

a Si cap layer under tensile strain on top of said top $Si_{1-m}Ge_m$ buffer layer,

wherein said relaxed bottom $Si_{1-z}Ge_z$ buffer layer, compressive-strained $Si_{1-v}Ge_v$ quantum well layer, top $Si_{1-m}Ge_m$ buffer layer and Si cap layer are substantially undoped.

23. (Original) The semiconductor layer structure as claimed in Claim 22, wherein said compressive-strained $Si_{1-v}Ge_v$ quantum well layer has a Ge concentration, v, such that $v > z + 0.3$.

24. (Original) The semiconductor layer structure as claimed in Claim 23, wherein the n-type portion of said relaxed $Si_{1-x}Ge_x$ layer has a dopant concentration between 10^{15} cm^{-3} and 10^{19} cm^{-3} and said relaxed $Si_{1-x}Ge_x$ layer has a Ge concentration x and relaxation, r, such that the in-plane lattice constant is 0-3.2% larger than that of bulk Si.

25. (Original) The semiconductor layer structure as claimed in Claim 24, wherein:

said bottom $Si_{1-z}Ge_z$ buffer layer is substantially lattice-matched to said relaxed $Si_{1-x}Ge_x$ layer and has a thickness ranging between 2 nm to 50 nm;

said compressive-strained $Si_{1-v}Ge_v$ quantum well layer has a thickness ranging between 2 nm to 30 nm;

said top $Si_{1-m}Ge_m$ buffer layer is substantially lattice-matched to said bottom $Si_{1-z}Ge_z$ buffer layer and has a thickness ranging between 2 nm to 30 nm; and,

said Si cap layer has a thickness ranging between 0 nm to 5 nm.

26. (Original) The semiconductor layer structure as claimed in Claim 25, wherein said relaxed $Si_{1-x}Ge_x$ layer is formed on top of an insulating layer.

27. (Currently Amended) A ~~The~~ semiconductor layer structure comprising: ~~as claimed in Claim 21,~~

a relaxed $Si_{1-x}Ge_x$ layer; wherein said relaxed $Si_{1-x}Ge_x$ layer is doped either partially or wholly n-type,

a bottom $Si_{1-z}Ge_z$ buffer layer on top of said relaxed $Si_{1-x}Ge_x$ layer;

a compressive-strained $Si_{1-v}Ge_v$ quantum well layer on top of said bottom $Si_{1-z}Ge_z$ buffer layer;

a top $Si_{1-m}Ge_m$ buffer layer on top of said compressive-strained Si quantum well layer;

a Si cap layer under tensile strain on top of said top $Si_{1-m}Ge_m$ buffer layer,

wherein a portion of said bottom $Si_{1-z}Ge_z$ buffer layer or top $Si_{1-m}Ge_m$ buffer layer or both buffer layers adjacent to said $Si_{1-v}Ge_v$ quantum well layer is substantially undoped and a portion or entirety of the remaining regions of said bottom $Si_{1-z}Ge_z$ buffer layer or top $Si_{1-m}Ge_m$ buffer layer or both buffer layers is doped p-type with a concentration ranging between $10^{17}cm^{-3}$ to 10^{21} cm^{-3}.

28. (Original) The semiconductor layer structure as claimed in Claim 27, where the thickness of the undoped portion of said bottom $Si_{1-z}Ge_z$ buffer layer or top $Si_{1-m}Ge_m$ buffer layer or both buffer layerS adjacent to said $Si_{1-v}Ge_v$ quantum well is at least 0.5 nm.

29. (Original) The semiconductor layer structure as claimed in Claim 28, wherein said compressive-strained $Si_{1-v}Ge_v$ quantum well layer has a Ge concentration, v, such that $v > z + 0.3$.

30. (Original) The semiconductor layer structure as claimed in Claim 29, wherein the n-type portion of said relaxed $Si_{1-x}Ge_x$ layer has a dopant concentration between 10^{15} cm^{-3} and 10^{19} cm^{-3} and said relaxed $Si_{1-x}Ge_x$ layer has a Ge concentration x and relaxation, r, such that the in-plane lattice constant is 0-3.2% larger than that of bulk Si.

31. (Original) The semiconductor layer structure as claimed in Claim 30, wherein:

said bottom $Si_{1-z}Ge_z$ buffer layer is substantially lattice-matched to said relaxed $Si_{1-x}Ge_x$ layer and has a thickness ranging between 2 nm to 50 nm;

said compressive-strained $Si_{1-v}Ge_v$ quantum well layer has a thickness ranging between 2 nm to 30 nm;

said top $Si_{1-m}Ge_m$ buffer layer is substantially lattice-matched to said bottom $Si_{1-z}Ge_z$ buffer layer and has a thickness ranging between 2 nm to 30 nm; AND,

said Si cap layer has a thickness ranging between 0 nm to 5 nm.

32. (Original) The semiconductor layer structure as claimed in Claim 31, wherein said relaxed $Si_{1-x}Ge_x$ layer is formed on top of an insulating layer.

33. (Canceled)

34. (Currently Amended) A semiconductor layer structure comprising: ~~as claimed in Claim 33,~~

a relaxed $Si_{1-x}Ge_x$ layer; wherein said relaxed $Si_{1-x}Ge_x$ layer is doped either partially or wholly n-type,

an interposer $Si_{1-y}Ge_y$ layer on top of said relaxed $Si_{1-x}Ge_x$ layer;

a bottom $Si_{1-z}Ge_z$ buffer layer on top of said interposer $Si_{1-y}Ge_y$ layer;

a compressive-strained $Si_{1-v}Ge_v$ quantum well layer on top of said bottom $Si_{1-z}Ge_z$ buffer layer;

a top $Si_{1-m}Ge_m$ buffer layer on top of said compressive-strained Si quantum well layer;

a Si cap layer under tensile strain on top of said top $Si_{1-m}Ge_m$ buffer layer,

wherein said relaxed bottom $Si_{1-z}Ge_z$ buffer layer, compressive-strained $Si_{1-v}Ge_v$ quantum well layer, top $Si_{1-m}Ge_m$ buffer layer and Si cap layer are substantially undoped.

35. (Original) The semiconductor layer structure as claimed in Claim 34, wherein said compressive-strained $Si_{1-v}Ge_v$ quantum well layer has a Ge concentration, v, such that $v > z+0.3$.

36. (Original) The semiconductor layer structure as claimed in Claim 35, wherein the n-type portion of said relaxed $Si_{1-x}Ge_x$ layer has a dopant concentration between 10^{15} cm^{-3} and 10^{19} cm^{-3} and said relaxed $Si_{1-x}Ge_x$ layer has a Ge concentration x and relaxation, r, such that the in-plane lattice constant is 0-3.2% larger than that of bulk Si.

37. (Original) The semiconductor layer structure as claimed in Claim 36, wherein:

said interposer $Si_{1-y}Ge_y$ layer has Ge concentration, y, in the range of 0 to 20%, and thickness less than 5 nm;

said bottom $Si_{1-z}Ge_z$ buffer layer is substantially lattice-matched to said relaxed $Si_{1-x}Ge_x$ layer and has a thickness ranging between 2 nm to 50 nm;

said compressive-strained $Si_{1-v}Ge_v$ quantum well layer has a thickness ranging between 2 nm to 30 nm;

said top $Si_{1-m}Ge_m$ buffer layer is substantially lattice-matched to said bottom $Si_{1-z}Ge_z$ buffer layer and has a thickness ranging between 2 nm to 20 nm; and,

said Si cap layer has a thickness ranging between 0 nm to 5 nm.

38. (Original) The semiconductor layer structure as claimed in Claim 37, wherein said relaxed $Si_{1-x}Ge_x$ layer is formed on top of an insulating layer.

39. (Currently Amended) ~~The~~ A semiconductor layer structure comprising: ~~as claimed in Claim 33,~~

a relaxed $Si_{1-x}Ge_x$ layer; wherein said relaxed $Si_{1-x}Ge_x$ layer is doped either partially or wholly n-type,

an interposer $Si_{1-y}Ge_y$ layer on top of said relaxed $Si_{1-x}Ge_x$ layer;

a bottom $Si_{1-z}Ge_z$ buffer layer on top of said interposer $Si_{1-y}Ge_y$ layer;

a compressive-strained $Si_{1-v}Ge_v$ quantum well layer on top of said bottom $Si_{1-z}Ge_z$ buffer layer;

a top $Si_{1-m}Ge_m$ buffer layer on top of said compressive-strained Si quantum well layer;

a Si cap layer under tensile strain on top of said top $Si_{1-m}Ge_m$ buffer layer,

wherein a portion of said bottom $Si_{1-z}Ge_z$ buffer layer or top $Si_{1-m}Ge_m$ buffer layer or both buffer layers adjacent to said $Si_{1-v}Ge_v$ quantum well layer is substantially undoped and a portion or entirety of the remaining regions of said bottom $Si_{1-z}Ge_z$ buffer layer or top $Si_{1-m}Ge_m$ buffer layer or both buffer layers is doped p-type with a concentration ranging between $10^{17}cm^{-3}$ to 10^{21} cm^{-3}.

40. (Original) The semiconductor layer structure as claimed in Claim 39, where the thickness of the undoped portion of said bottom $Si_{1-z}Ge_z$ buffer layer or top $Si_{1-m}Ge_m$ buffer layer or both buffer layers adjacent to said $Si_{1-v}Ge_v$ quantum well is at least 0.5 nm.

41. (Original) The semiconductor layer structure as claimed in Claim 40, wherein said compressive-strained $Si_{1-v}Ge_v$ quantum well layer has a Ge concentration, v, such that $v > z+0.3$.

42. (Original) The semiconductor layer structure as claimed in Claim 41, wherein the n-type portion of said relaxed $Si_{1-x}Ge_x$ layer has a dopant concentration between 10^{15} cm^{-3} and 10^{19} cm^{-3} and said relaxed $Si_{1-x}Ge_x$ layer has a Ge concentration x and relaxation, r, such that the in-plane lattice constant is 0-3.2% larger than that of bulk Si.

43. (Original) The semiconductor layer structure as claimed in Claim 42, wherein:

said interposer $Si_{1-y}Ge_y$ layer has Ge concentration, y, in the range of 0 to 20%, and thickness less than 5 nm;

said bottom $Si_{1-z}Ge_z$ buffer layer is substantially lattice-matched to said relaxed

$Si_{1-x}Ge_x$ layer and has a thickness ranging between 2 nm to 50 nm;

said compressive-strained $Si_{1-v}Ge_v$ quantum well layer has a thickness ranging between 2 nm to 30 nm;

said top $Si_{1-m}Ge_m$ buffer layer is substantially lattice-matched to said bottom $Si_{1-z}Ge_z$ buffer layer and has a thickness ranging between 2 nm to 20 nm.

44. (Original) The semiconductor layer structure as claimed in Claim 39, wherein said relaxed $Si_{1-x}Ge_x$ layer is formed on top of an insulating layer.

Claims 45-57 (Canceled)

58. (Currently Amended) The semiconductor layer structure as claimed in Claim [[1]] 2, further comprising:

an insulating gate dielectric located on top of said Si cap layer;

a gate electrode located on top of said insulating gate dielectric;

n-type source and drain contact regions located on either side of said gate electrode, and extending from a surface of said structure down to the p-type doped portion of said relaxed

$Si_{1-x}Ge_x$ layer;

trench isolation regions on either side said drain and source contact regions that penetrate into said relaxed $Si_{1-x}Ge_x$ layer, whereby a high-performance field effect transistor device results.

59. (Currently Amended) The semiconductor layer structure as claimed in Claim ~~11~~ 12, further comprising:

an insulating gate dielectric located on top of said Si cap layer;

a gate electrode located on top of said insulating gate dielectric;

n-type source and drain contact regions located on either side of said gate electrode, and extending from a surface of said structure down to the p-type doped portion of said relaxed

$Si_{1-x}Ge_x$ layer;

trench isolation regions on either side said drain and source contact regions that penetrate into said relaxed $Si_{1-x}Ge_x$ layer, whereby a high-performance field effect transistor device results.

60. (Original) The semiconductor layer structure as claimed in Claim 6, further comprising:

a gate electrode located on top of said Si cap layer;

n-type source and drain contact regions located on either side of said gate electrode, and extending from a surface of said structure down to the p-type doped portion of said relaxed $Si_{1-x}Ge_x$ layer;

trench isolation regions on either side said drain and source contact regions that penetrate into said relaxed $Si_{1-x}Ge_x$ layer, whereby a high-performance field effect transistor device results.

61. (Original) The semiconductor layer structure as claimed in Claim 60, further comprising an insulating gate dielectric located on top of said Si cap layer and below said gate electrode.

62. (Original) The semiconductor layer structure as claimed in Claim 16, further comprising:

a gate electrode located on top of said Si cap layer;

n-type source and drain contact regions located on either side of said gate electrode, and extending from a surface of said structure down to the p-type doped portion of said relaxed $Si_{1-x}Ge_x$ layer;

trench isolation regions on either side said drain and source contact regions that penetrate into said relaxed $Si_{1-x}Ge_x$ layer, whereby a high-performance field effect transistor device results.

63. (Original) The semiconductor layer structure as claimed in Claim 62, further comprising an insulating gate dielectric located on top of said Si cap layer and below said gate electrode.

64. (Original) The semiconductor layer structure as claimed in Claim 5, further comprising:

an insulating gate dielectric located on top of said Si cap layer;

a gate electrode located on top of said insulating gate dielectric;

n-type source and drain contact regions located on either side of said gate electrode, and extending from a surface of said structure down to said insulating layer;

trench isolation regions on either side of drain and source contact regions that penetrate through said relaxed $Si_{1-x}Ge_x$ layer, and into said insulating layer.

65. (Original) The semiconductor layer structure as claimed in Claim 15, further comprising:

an insulating gate dielectric located on top of said Si cap layer;

a gate electrode located on top of said insulating gate dielectric;

n-type source and drain contact regions located on either side of said gate electrode, and extending from a surface of said structure down to said insulating layer;

trench isolation regions on either side of drain and source contact regions that penetrate through said relaxed $Si_{1-x}Ge_x$ layer, and into said insulating layer.

66. (Original) The semiconductor layer structure as claimed in Claim 10, further comprising:

a gate electrode located on top of said Si cap layer;

n-type source and drain contact regions located on either side of said gate electrode, and extending from a surface of said structure down to said insulating layer;

trench isolation regions on either side of drain and source contact regions that penetrate through said relaxed $Si_{1-x}Ge_x$ layer, and into said insulating layer.

67. (Original) The semiconductor layer structure as claimed in Claim 66, further comprising an insulating gate dielectric located on top of said Si cap layer and below said gate electrode.

68. (Original) The semiconductor layer structure as claimed in Claim 20, further comprising:

a gate electrode located on top of said Si cap layer;

n-type source and drain contact regions located on either side of said gate electrode, and extending from a surface of said structure down to said insulating layer;

trench isolation regions on either side of drain and source contact regions that penetrate through said relaxed $Si_{1-x}Ge_x$ layer, and into said insulating layer.

69. (Original) The semiconductor layer structure as claimed in Claim 68, further comprising an insulating gate dielectric located on top of said Si cap layer and below said gate electrode.

70. (Currently Amended) The semiconductor layer structure as claimed in Claim ~~21~~ 22, further comprising:

an insulating gate dielectric located on top of said Si cap layer;

a gate electrode located on top of said insulating gate dielectric;

p-type source and drain contact regions located on either side of said gate electrode, and extending from a surface of said structure down to the p-type doped portion of said relaxed $Si_{1-x}Ge_x$ layer;

trench isolation regions on either side said drain and source contact regions that penetrate into said relaxed $Si_{1-x}Ge_x$ layer, whereby a high-performance field effect transistor device results.

71. (Currently Amended) The semiconductor layer structure as claimed in Claim ~~33~~ 34, further comprising:

an insulating gate dielectric located on top of said Si cap layer;

a gate electrode located on top of said insulating gate dielectric;

p-type source and drain contact regions located on either side of said gate electrode, and extending from a surface of said structure down to the p-type doped portion of said relaxed $Si_{1-x}Ge_x$ layer;

trench isolation regions on either side said drain and source contact regions that penetrate into said relaxed $Si_{1-x}Ge_x$ layer, whereby a high-performance field effect transistor device results.

72. (Original) The semiconductor layer structure as claimed in Claim 27, further comprising:

a gate electrode located on top of said Si cap layer;

p-type source and drain contact regions located on either side of said gate electrode, and extending from a surface of said structure down to the p-type doped portion of said relaxed $Si_{1-x}Ge_x$ layer;

trench isolation regions on either side said drain and source contact regions that penetrate into said relaxed $Si_{1-x}Ge_x$ layer, whereby a high-performance field effect transistor device results.

73. (Original) The semiconductor layer structure as claimed in Claim 72, further comprising an insulating gate dielectric located on top of said Si cap layer and below said gate electrode.

74. (Original) The semiconductor layer structure as claimed in Claim 39, further comprising:

a gate electrode located on top of said Si cap layer;

p-type source and drain contact regions located on either side of said gate electrode, and extending from a surface of said structure down to the p-type doped portion of said relaxed $Si_{1-x}Ge_x$ layer;

trench isolation regions on either side said drain and source contact regions that penetrate into said relaxed $Si_{1-x}Ge_x$ layer, whereby a high-performance field effect transistor device results.

75. (Original) The semiconductor layer structure as claimed in Claim 74, further comprising an insulating gate dielectric located on top of said Si cap layer and below said gate electrode.

76. (Original) The semiconductor layer structure as claimed in Claim 26, further comprising:

an insulating gate dielectric located on top of said Si cap layer;

a gate electrode located on top of said insulating gate dielectric;

p-type source and drain contact regions located on either side of said gate electrode, and extending from a surface of said structure down to said insulating layer;

trench isolation regions on either side of drain and source contact regions that penetrate through said relaxed $Si_{1-x}Ge_x$ layer, and into said insulating layer.

77. (Original) The semiconductor layer structure as claimed in Claim 38, further comprising:

an insulating gate dielectric located on top of said Si cap layer;

a gate electrode located on top of said insulating gate dielectric;

p-type source and drain contact regions located on either side of said gate electrode, and extending from a surface of said structure down to said insulating layer;

trench isolation regions on either side of drain and source contact regions that penetrate through said relaxed $Si_{1-x}Ge_x$ layer, and into said insulating layer.

78. (Original) The semiconductor layer structure as claimed in Claim 32, further comprising:

a gate electrode located on top of said Si cap layer;

p-type source and drain contact regions located on either side of said gate electrode, and extending from a surface of said multi-layer structure down to said buried oxide layer;

trench isolation regions on either side of drain and source contact regions that penetrate through said relaxed $Si_{1-x}Ge_x$ layer, and into said insulating layer.

79. (Original) The semiconductor layer structure as claimed in Claim 78, further comprising an insulating gate dielectric located on top of said Si cap layer and below said gate electrode.

80. (Original) The semiconductor layer structure as claimed in Claim 44, further comprising:

a gate electrode located on top of said Si cap layer;

p-type source and drain contact regions located on either side of said gate electrode, and extending from a surface of said multi-layer structure down to said buried oxide layer;

trench isolation regions on either side of drain and source contact regions that penetrate through said relaxed $Si_{1-x}Ge_x$ layer, and into said insulating layer.

81. (Original) The semiconductor layer structure as claimed in Claim 80, further comprising an insulating gate dielectric located on top of said Si cap layer and below said gate electrode.

82. (Original) The semiconductor layer structure as claimed in Claim 58, wherein said insulating gate dielectric comprises one selected from the group comprising: an oxide, nitride, oxynitride of silicon, and oxides and silicates of Hf, Al, Zr, La, Y, Ta, singly or in combinations and the bottom portion of said gate electrode comprises polysilicon, polysilicongermanium, or the metals: Mo, Pt, Ir, W, Pd, Al, Au, Ni, Cu, Ti, and Co or their silicides and germanosilicides, either singly or in combinations.

83. (Original) The semiconductor layer structure as claimed in Claim 59, wherein the bottom portion of said gate electrode comprises one selected from the group comprising: polysilicon, polysilicongermanium, or metals: Pt, Ir and Pd or their silicides and germanosilicides, either singly or in combinations.

84. (Original) The semiconductor layer structure as claimed in Claim 65, wherein the bottom portion of said gate electrode comprises one selected from the group comprising: polysilicon, polysilicongermanium, or metals: Mo, W, Al, Au, Ni, Cu, Ti, and Co or their silicides and germanosilicides, either singly or in combinations.